

Evaluation of Microprocessor

The first microprocessor introduced in 1971 was a 4-bit microprocessor with 4m5KB memory and had a set of 45 instructions. In the past 5 decades microprocessor speed has doubled every two years, as predicted by Gordon Moore, Intel co-founder. Current microprocessors can access 64GB memory. Depending on width of data microprocessors can process, they are of these categories -

- 8-bit
- 16-bit
- 32-bit
- 64-bit

Size of Instructions set is another important consideration while categorizing microprocessor. Initially, microprocessors had very small instructions sets because complex hardware was expensive as well as difficult to build.

As technology developed to overcome these issues, more and more complex instructions were added to increase functionality of the microprocessor. However, soon it was realized that having large instructions sets was counterproductive as many instructions that were rarely used sat idle on ~~pro~~ precious memory space. So the old school of thought that supported smaller instruction sets gained popularity.

Name	Year	Transistors	Data width	clock speed
8080	1974	6,000	8 bits	2 MHz
8085	1976	6,500	8 bits	5 MHz
8086	1978	29,000	16 bits	5 MHz
8088	1979	29,000	8 bits	5 MHz
80286	1982	134,000	16 bits	6 MHz
80386	1985	275,000	32 bits	16 MHz
80486	1989	1,200,000	32 bits	25 MHz
PENTIUM	1993	3,100,000	32/64 bits	60 MHz
PENTIUM II	1997	7,500,000	64 bits	233 MHz
PENTIUM III	1999	9,500,000	64 bits	450 MHz
PENTIUM IV	2000	42,000,000	64 bits	1.5 GHz

Microprocessor - 8085 :-

8085 is pronounced as "eighty-eighty-five" microprocessor. It is an 8-bit microprocessor designed by Intel in 1977 using NMOS technology.

- 8-bit data Bus
- 16-bit address bus, which can address up to 64 Kb.
- A 16-bit program counter
- A 16-bit stack pointer
- 8-bit registers arranged in pairs:
- BC, DE, HL.
- Requires +5V supply to operate at 3.2 MHz single phase clock. It is used in washing machines, microwaves ovens, mobile phone, etc.

8085 Microprocessor - Functional Units :-

- 1- Accumulator :- It is an 8-bit register used to perform arithmetic, logical, I/O and load/store operations. It is connected to internal data bus and ALU.

- 2- Arithmetic and Logic unit :- As the name suggests, it performs arithmetic and logical operations like Addition, Subtraction, AND, OR, etc. on 8-bit data.
- 3- General purpose register :- There are 6 general purpose registers in 8085 processor i.e. B, C, D, E, H and L. Each register can hold 8-bit data. These registers can work in pairs to hold 16-bit data and their pairing combination is like B-C, D-E and H-L.
- 4- Program Counter :- It is a 16-bit register used to store the memory address location of the next instruction to be executed. Microprocessor increments the program whenever an instruction is being executed, so that the program counter points to the memory address of the next instruction that is going to be executed.
- 5- Stack pointer :- It is also a 16-bit register works like stack, which is always incremented/decremented by 2 during push

and pop operations.

6- Temporary register :- It is 8-bit register which hold the temporary data of arithmetic and logical operations.

7- Flag register - It is an 8-bit register having five 1-bit flip-flop which hold either 0 or 1 depending upon the result stored in the accumulator.

i) Sign (S).

ii) Zero (Z).

iii) Auxiliary carry (AC)

iv) Parity (P)

v) Carry (C).

Its bit position is shown in the following table-

D7	D6	D5	D4	D3	D2	D1	D0
S	Z	AC	P	CY			

8- Instruction register and decoder -

It provides timing and control signal to the microprocessor to perform

operations. Following are the timing and control signals, which control external and internal circuits - control signals -

READY, RD', WR', ALE

Status signals - SO, SI, IO/M'

DMA signals - HOLD, HLDA

RESET signals - RESET IN, RESET OUT.

10- Interrupt Control - As the name suggests it controls the interrupts during a process. When a microprocessor is executing a main program an interrupt occurs, the microprocessor shifts the control from the main program to process the incoming requests. After the request is completed, the control goes back to the main program.

There are 5 interrupt signals in 8085 microprocessor - INTR, RST 7.5, RST 6.5, RST 5.5, TRAP.

11- Serial Input/Output Control - It controls the serial data communication by using these two instructions -

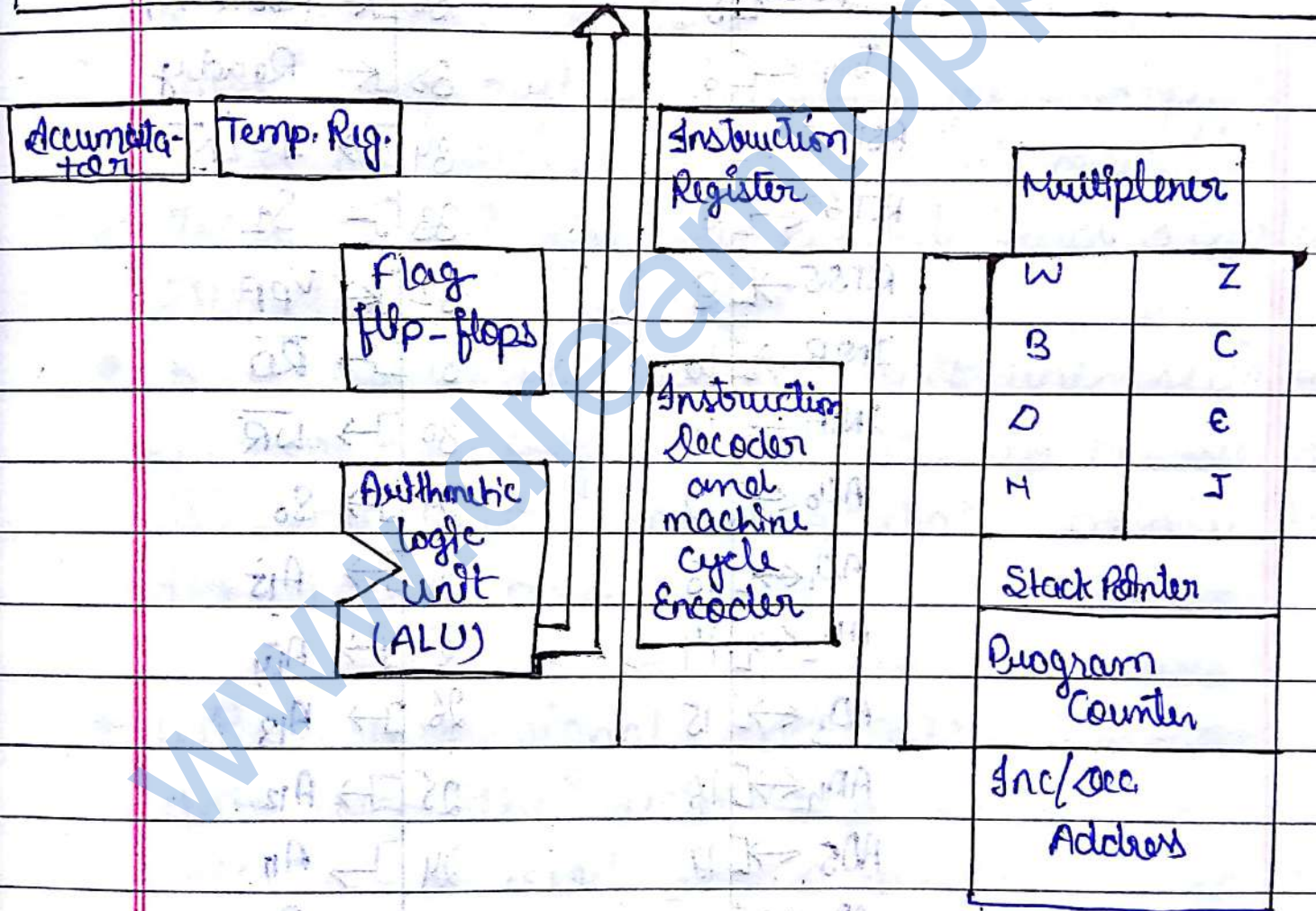
- (i) SID (Serial Input data)
- (ii) SOD (Serial Output data).

12- Address buffer and address-data buffer -
The content stored in the stack pointer and program counter is loaded into the address buffer and address-data buffer to communicate with the connected CPU.

The memory and I/O chips are connected to these buses, the CPU can exchange the desired data with the memory and I/O chips.

13- Address bus and data bus - Data bus carries the data to be stored. It is bidirectional, whereas address bus carries the location to where it should be stored and it is unidirectional. It is used to transfer the data and address I/O devices.

★ 8085 Architecture -



The following figure depicts the pin diagram of 8085 microprocessor -

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$X_1 \rightarrow$	1	40	V_{CC}
$X_2 \rightarrow$	2	39	\overline{HOLD}
Out \leftarrow	3	38	$HOLDA$
SOO \leftarrow	4	37	$CLK(out)$
SIO \rightarrow	5	36	$\overline{Reset In}$
Trap \leftarrow	6	35	Ready
RST 7.5 \rightarrow	7	34	IO/\overline{M}
RST 6.5 \leftarrow	8	33	S_1
RST 5.5 \rightarrow	9	32	V_{PP}
INTR \rightarrow	10	31	\overline{RD}
INTA \leftarrow	11	30	\overline{WR}
$AD_0 \leftrightarrow$	12	29	S_0
$AD_1 \leftrightarrow$	13	28	A_{15}
$AD_2 \leftrightarrow$	14	27	A_{14}
$AD_3 \leftrightarrow$	15	26	A_{13}
$AD_4 \leftrightarrow$	16	25	A_{12}
$AD_5 \leftrightarrow$	17	24	A_{11}
$AD_6 \leftrightarrow$	18	23	A_{10}
$AD_7 \leftrightarrow$	19	22	A_9
$V_{SS} \leftrightarrow$	20	21	A_8

The pin of a 8085 microprocessor can be classified into seven groups -

- 1- Address bus - $A_{15} - A_8$, It carries the most significant 8-bits of memory / IO address.
- 2- Data bus - ~~AD~~ $AD_7 - AD_0$, It carries the least significant 8-bit address and data bus.
- 3- Control and Status signals - These signals are used to identify the nature of operation. There are 3 Control signal and 3 Status signals.
 - RD - This signal indicates that the selected IO or memory device is to be read and is ready for accepting data available on the data bus.
 - WR - This signal indicates that the data on the data bus is to be written into a selected memory or IO location.
 - ALE - It is a positive going pulse generated when a new operation is starting in the microprocessor. When the pulse goes high, it indicates address; when the pulse goes down it indicates data.

Three status signals are IO/M, SO & S1.

1- IO/M - This signal is used to differentiate between IO and memory operations, i.e. when it is high it indicates IO operation and when it is low then it indicates memory operation.

2- S1 & S0 - These signals are used to identify the type of current operation.

3- Power Supply - There are two power supply signals - VCC & VSS indicates +5V power supply and it indicates ground signal.

Clock signals - There are 3 clock signals - i.e. X1, X2, CLK OUT.

- X1, X2 - A crystal (RC, LC NIW) is connected at these two pins and is used to set frequency of the internal clock generator. This frequency is internally divided by 2.

- **CLK Out** :- This signal is used as the system clock for devices connected with the microprocessor.
- ★ **Interrupts & externally initiated signals** :- Interrupt are the signals generated by external devices to request the microprocessor to perform a task. There are 5 interrupt signals, i.e. TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR.
- **INTA** - It is an interrupt acknowledgement signal.
- **RESET IN** - This signal is used to reset the microprocessor by setting the program counter to zero.
- **RESET OUT** - This signal is used to reset all the connected devices when the microprocessor is reset.
- **READY** :- This signal indicates that the device is ready to send or receive data. If READY is low, then the CPU has to wait for READY to go high.
- **HOLD** - This signal indicates that another master is requesting the use of address and data buses.

- **HOLD (Hold Acknowledgement)** - It indicates that the CPU has received the HOLD request and it will relinquish the bus in the next clock cycle. HOLD is set to low after the HOLD signal is removed.

7. **Serial I/O signals**:- There are 2 serial signals, i.e. SID and SOD and these signals are used for serial communication.

- **SOD (Serial Output data line)**:- The output SOD is set/reset as specified by the SIM instruction.

- **SID (Serial Input data line)**:- The data on this line is loaded into accumulator whenever a RIM instruction is executed.

* **Addressing Modes in 8085**:-

These are the instructions used to transfer the data from one register to another register, from the memory to the register, and from the register to

the memory without any alteration in the content. Addressing modes in 8085 is classified into 5 groups -

- 1- Immediate addressing mode - In this mode, the 8/16 bit data is specified in the instruction itself as one of its operand. For example:-
MOV K, 20F: means 20F is copied into register K.
- 2- Register addressing mode - In this mode, the data is copied from one register to another. For example:-
MOV K, B: means data in register B is copied to register K.
- 3- Direct addressing mode - In this mode, the data is directly copied from the given address to the register. For example:-
LDB 5000K: means the data at address 5000K is copied to register B.
- 4- Indirect addressing mode - In this mode, the data is transferred from one register to another by using the address pointed

by the register.

For ex - MOV K, B: means data is transferred from the memory address pointed by the register to the register K.

5- Implied addressing mode - This mode does not require any operand, the data is specified by the opcode itself.
For ex - CMP.

* Interrupts In 8085:-

Interrupts are the signals generated by the external devices to request the microprocessor to perform a task. There are 5 interrupt signals, i.e. TRAP, RST 6.5, RST 7.5, RST 5.5 and INTR.

Interrupt are classified into following groups based on their parameter -

1- Vector Interrupt - In this type of interrupt the interrupt address is known to the processor.

For ex:- RST 5.5, RST 6.5, RST 7.5, TRAP.

2- Non-Vector Interrupt - In this type of interrupt, the interrupt is not known to the processor, so, the interrupt address needs to be sent externally by the device to perform interrupts. For ex - INTR.

3 Markable Interrupt :- In this type of interrupt, we can disable the interrupt by writing some instructions into the program. For example: RST 7.5, RST 6.5, RST 5.5.

4 Non-Markable interrupt :- In this type of interrupt we cannot disable the interrupt by writing some instructions into the program. For example: TRAP.

5- Software Interrupt :- In this type of interrupt, the programmer has to add the instructions into the program to execute the interrupt. There are 8 software interrupts in 8085, i.e. RST 0, RST 1, RST 2, RST 3, RST 4, RST 5, RST 6, and RST 7.

6-● Hardware Interrupt :- There are 5 interrupts pins in 8085 used as hardware interrupt, i.e., TRAP, RST 7.5, RST 6.5, RST 5.5, INTA.

NOTE :- INTA is not an interrupt, it is used by the microprocessor for sending acknowledgement. TRAP has the highest priority, then RST 7.5 and so on.

● Interrupt Service Routine (ISR) :- A small program or a routine that when executed, services the corresponding interrupting source is called an ISR.

A. TRAP :-

It is a non-maskable interrupt, having the highest priority among all interrupts. By default, it is enabled until it gets acknowledged.

In case of failure, it executes as ISR and sends the data to backup memory. This interrupt transfers the control to the location 0024H.

RST 7.5° - It is a maskable interrupt, having the second highest priority among all interrupts. When this interrupt is executed, the processor saves the content of the PC register into the stack and branches to 003CH address.

RST 6.5° - It is a maskable interrupt, having the third highest priority among all interrupts. When this interrupt is executed the processor saves the content of the PC register into the stack and branches to 0034H address.

RST 5.5° - It is a maskable interrupt. When this interrupt is executed, the processor saves the content of the PC register into the stack and branches to 002CH address.

INTR° - It is a maskable interrupt, having the lowest priority among all interrupts. It can be disabled by resetting the microprocessor.

- When INTR signal goes high, the following event can occur -

- The microprocessor checks the status of INTR signal during the execution of each instruction.
- When the INTR signal is high, then the microprocessor saves the address of the next instruction to complete its current instructions and sends active low interrupt acknowledge signal.
- When instructions are received, then the microprocessor saves the address of the next instruction on stack and executes the received instruction.